(BTM) Model is an equivalent circuit that represents the AC charecterstics of the transistors . It uses circuit elements that approximate the behaviour of the transistors. re model , Hybrid equivalent model . B to E || C to E**C to B** -> Emitter internal , AC analysis : is used to calculate the small-signal response of a circuit. Capacitor shot , DC source GRND -> C to E internal

re=26mv/IE Av=(Rc||ro)/re (Zo/Zi)

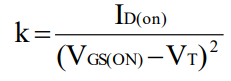
Transistor(3 terminal) is a semiconductor device that is used to amlify or as switch.(2types1) 1. FET : Field effect 2. BJT : (Bipolar Junction ) (Two polarity ) (NPN,PNP) (BASE,COLLECTOR,EMITTER) BJT : Fixed Bias, Emitter Bias, Voltage Dovider , Collector

Device (2types) BIPOLAR,(current will flow for both holes and electrones) UNIPOLAR(Current will only flow for Holes or Electron) Less sensitive = Temp change but char change hoy na temon

**FET** -> **JFET(**Junction Field Effect Transistor**)** **(2 type N,P) (**3 terminal-> **get,dren** ,**sources)**, **MOSFET(Metal Oxide Semiconductor field effect transistor) (**4 terminal **get**,**dren** ,**source** ,**body) (2 typye D,E) (N,P)**

FET(**voltage control**,**unipolar** ,**size kom** ,**use beshi**,**cost besi**,) **VS** BJT( **current base technical control**,**bipolar**,**size beshi** ,**use kom**,**cost kom**)

JFET : G,D,S ID=IDSS(1-VGS/VP)^2 IDSS ? **0.3Vp=Idss/2** **0.5Vp=Idss/4** **Vp=0ma**

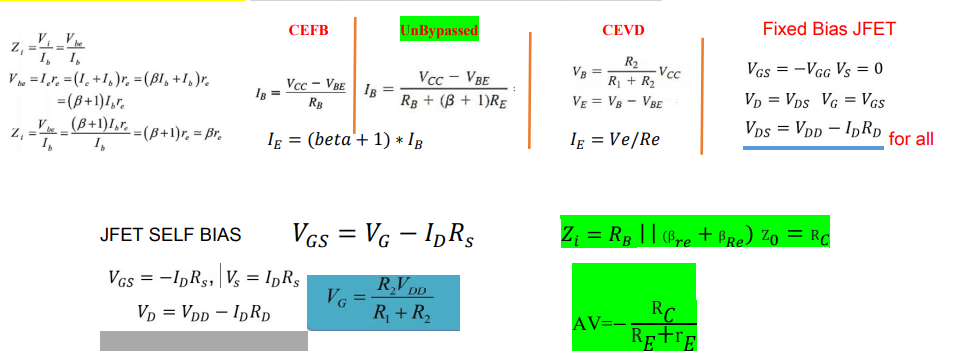
MOSFET :G,D,S,B(Gate voltage apply করলে Current Flow হবে Positive ion কে elctron attarct করবে এবং elecrton উপরের দিক চলে যেয়ে channel create করে .   ID vs Vds with with respect to Vgs

D mosfate= initally channel is create. Jetar maddome current flow kore .

E mosfate= no initally channel is create,current will flow we will apply get voltage .

For JFET & MOSFET => ID=IS , IG=0 (Gate এ High input impdence এর কারণে Current flow হয় না তাই Full current Drain থেকে source যাবে )

CMOS: Complementary MOSFET that has both p-channel and n-channel in the same substrate . Apply 1 get 0 Apply 0 get 1 যত গুলো P Chnl ততগুলো N যত গুলো N Chnl ততগুলো P

DC Analysis /Load Line Analysis: Capacitor Open thake . kno Ac signal present thake na .Q point নির্ণয় করি

JFET

fixed: ekta source voltage deya thakbe jeta fixed.

>vds(use kvl ,dc analysis kora lage)= -vdd+IdRd+vgs; vs=0; vD= vds;



**Slef: >kno source voltage thakbe na ,**

**Is=id; ig=0; +vgs+IsRs ba +vgs+IdRs;**



****

**>Prothome origin ber korte hbe ,**



**>vgs er pointer jonno Id ber krte hbe .tr por q point ber korbo.**



Voltage divider bias:



>Vdd is separate into two equvalent souces;

>mul binddu gami sorol rekhan hbe na .

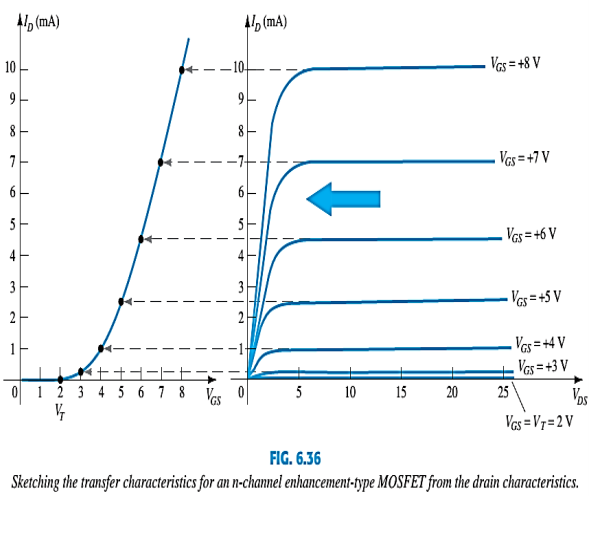
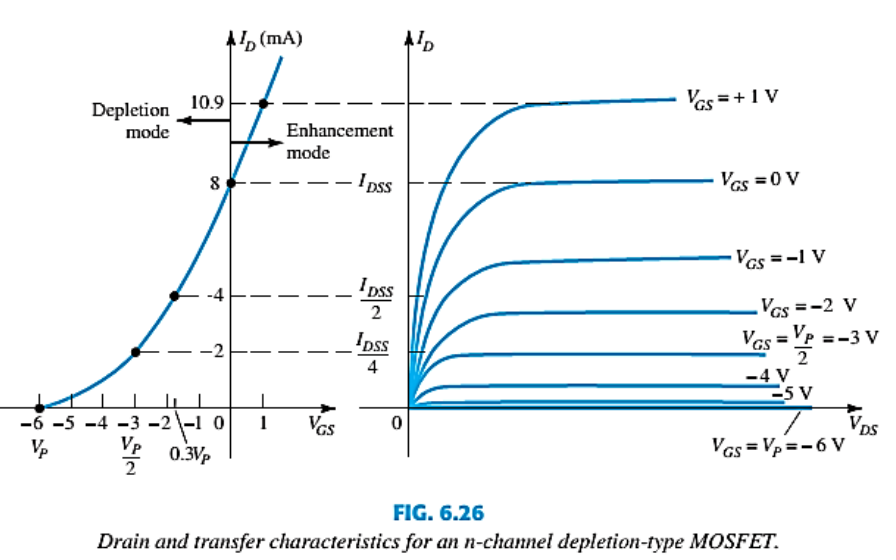
>Vg=R2\*vD/(R1+R2); -Vg+Vgs+IsRs=0; Id=1/Rs(-vgs) +vg/Rs

D mosfae> same as JFET.

E mosfate>just id =k(vgs-vt)2 ;K=Id(on) /(vgs(on)-Vgs(th))2;

Tr por vg prime ber korbo ,tr por vgs=vg prime -Id Rs

**N-D ID VS VGS (-) | ID VS VDS (+) N-E ID VS VGS (-) | ID VS VDS (+)**



**P-D ID VS VGS (+) P-E ID VS VGS (-)**

